REMARKS

Claims 1-5 and 7-45 are pending in the application.

Claims 1-45 have been rejected.

Claims 1, 7, 8, 16, 26, 28, 34, 36, 38, and 44 have been amended. No new matter has been added by these amendments. Support for these amendments can be found, at least, on pages 20-24 of the specification.

Claim 6 has been cancelled.

Objection to the Specification

The specification was objected to, due to the lack of serial numbers in the cross-reference to related application section. The specification has been amended to include the serial numbers of the related applications. Accordingly, Applicant believes that the objections have been overcome and that the incorporation of these related applications by reference is proper.

Claim Interpretation

The Examiner stated that "for purposes of examination the examiner has determined that the 'ASCII string' as claimed refers to a method of encoding coefficients for a polynomial that is being programmed using a hardware description language and that any 'string' of values used for such a purpose is functionally equivalent to an 'ASCII string." Office Action, page 3. Applicants respectfully disagree with this assertion. Applicant notes that "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (C.C.P.A. 1970). Accordingly, it is improper to ignore the term "ASCII" when interpreting the claims. Furthermore, Applicant disagrees with the assertion that any "string" is the functional equivalent of an ASCII string. An ASCII string is a string that includes ASCII characters, which are encoded according to specific rules. A non-ASCII string lacks these characteristics.

Rejection of Claims under 35 U.S.C. § 112

Claims 26 and 36 stand rejected under 35 U.S.C. § 112, first paragraph, as being unpatentable for failing to comply with the enablement requirement. Specifically, due to a typographical error, these claims erroneously recited a "Field Error Correction Decoder" instead of a "Forward Error Correction Decoder." This error has been corrected. Accordingly, Applicant asserts that this rejection is moot.

Claims 34 and 44 were rejected for reciting the "forward error correction circuitry," which the Examiner asserted did not have sufficient antecedent basis. This language has been removed from claims 34 and 44. Accordingly, Applicant asserts that this rejection is moot.

Rejection of Claims under 35 U.S.C. § 102

Claim 7 was rejected under 35 U.S.C. § 102(b) as being anticipated by Foxcroft, U.S. Patent No. 5,818,855 (hereinafter referred to as "Foxcroft"). Applicant respectfully traverses this rejection.

Foxcroft fails to anticipate, teach, or suggest: "producing one or more parallel equations in a hardware description language" and "merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit", as recited in claim 7.

The portions of Foxcroft that are cited as teaching "producing one or more parallel equations" show how a conventional general Galois Field multiplier and Galois Field multiplier 116 were implemented using a standard hardware description language conforming to IEEE Standard 1364-1995. Foxcroft, col. 8, lines 23-27. Foxcroft provides this example in order to show how the area reports for the two Galois Field multipliers differ from each other. Foxcroft, col. 9, line 34 - col. 10, line 55. Applicant notes that the mere presence of equations in a hardware description language neither teaches nor suggests a method for producing one or more parallel equations and merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit. Thus, while the cited portion of Foxcroft does show equations that are represented in a hardware description language, Foxcroft clearly does not teach or suggest "producing one or more parallel equations in a hardware description language," as recited in claim 1. Similarly, the cited portions of Fox do not teach or suggest

"merging the one or more parallel equations into a hardware description language implementation of a Galois Field circuit."

Applicant notes that claim 7 has been amended; however, this amendment was not necessary to overcome the cited art.

Claims 26 and 36 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tomizawa et al, U.S. Patent No. 5,574,717 (hereinafter referred to as "Tomizawa"). Applicant respectfully traverses this rejection.

Tomizawa fails to anticipate, teach, or suggest a Forward Error Correction (FEC) decoder coupled to the receive line section module, the FEC decoder for decoding FEC check bits in the SONET signal, wherein the FEC decoder comprises a first circuit that implements one or more parallel equations, and the one or more parallel equations are generated by simulating a serial circuit," as recited in amended claim 26.

Tomizawa recites, in part:

> The FEC processing circuit is constituted by shift registers and exclusive-or circuits so as to perform FEC processing generating a remainder of a polynomial division. Furthermore, in case of large code-word size, a special parallel processing scheme is employed. In order to realize parallel FEC processing circuits, a simplified matrix method is developed. We use a matrix whose input vector is a concatenation of vectors of incoming data stream and initial data of shift registers, and an output vector is data of shift registers after passing clocks. A matrix for m-clock (where m>1) is easily obtained from a one-clock matrix using property of cyclic codes. And matrix representation is directly related to a circuit configuration by modulo 2 Galois field algebra. Tomizawa, col. 4, lines 40-55.

> Hereafter, a third embodiment of the present invention is described with reference to FIG. 9 and FIG. 10. FIG. 9 shows a configuration of a serial FEC processing circuit for a (18880,18865) Hamming code, wherein notations of circuit components and numerals are equivalent to those of FIG. 6. Different from the circuit of FIG. 6, an input port of data stream is located at a side of the register c15 which corresponds to a progressing direction of clocks. A number of clocks to obtain check bits is 32752 in a circuit of FIG. 13. Relationship between numerals of two states: a state after one clock progressing and the initial state, as,

$$c'_1=i_1+c_{15},\ c'_2=c_1+c_{15}+i_1,\ \text{otherwise}\ c'_j=c_{j-1}\ (\text{where}\ 3\leq j\leq 15) \quad (6)$$

In a later state established 8 clocks after the initial state, data of the shift registers are represented as follows:

$c''_1=c_1+i_8$

$c''_j=c_{j+6}+c_{j+5}+i_{9-j}+i_{10-j}$ (where $2\leq j\leq 8$)

$c''_9=c_1+c_{15}+i_1$

$c''_k=c_{k-8}$ (where $10\leq k\leq 15$) (7)

FIG. 10 shows a configuration of an 8-parallel FEC processing circuit for the (18880,18865) Hamming code, wherein parts equivalent to those of FIG. 13 will be designated by the same numerals. Since a number of 32752 is divided clearly by 8, it is not necessary to add a dummy bit for clock consistency, and a resultant clock number for check bit creation is 4096 at 19.5 MHz speed. As similar to the aforementioned circuit of FIG. 5, a circuit of FIG. 10 comprises 15 shift registers, however, a number of exclusive-ors is 24, where a single 3-input-type exclusive-or is counted as 2. In FIG. 10, a serial-parallel conversion circuit `d` and a check bit writing circuit `CW` are interconnected with 15 shift registers and 24 exclusive-ors so as to realize the logical processing of FIG. 9 at a lower clock rate. If some restriction is provided in circuit configuration, it is possible to use either the second embodiment or third one selectively. Tomizawa, col. 9, lines 15-56.

Thus, the cited portions of Tomizawa describe FEC processing circuits that include shift registers and exclusive-or circuits. The FEC processing circuits are realized in parallel according to a matrix method.

The cited portions of Tomizawa clearly do not teach or suggest "a first circuit that implements one or more parallel equations," where "the one or more parallel equations are generated by simulating a serial circuit," as recited in amended claim 26. (In fact, the term "simulating" does not appear anywhere within Tomizawa.) For at least the foregoing reasons, claim 26 is patentable over the cited art. Claim 36 is patentable over the cited art for similar reasons.

Rejection of Claims under 35 U.S.C. § 103

Claims 1-6 and 8-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Foxcroft in view of Oskouy et al, U.S. Patent No. 5,673,279 (hereinafter referred to as "Oskouy"), in further view of Kao, U.S. Patent No. 5,642,367 (hereinafter referred to as "Kao"). Applicant respectfully traverses this rejection.

The cited art fails to teach or suggest:

> "implementing a serial circuit representing the complex polynomial equation in a software program; wherein implementing the serial circuit includes
> storing a plurality of ASCII strings in each of a plurality of storage elements, wherein the plurality of ASCII strings represent a plurality of initial values of the serial circuit,
> storing one or more ASCII strings in each of one or more data structures wherein the one or more ASCII strings represent one or more mathematical operations in the serial circuit, and
> simulating the serial circuit to produce a plurality of parallel equations, wherein simulating the serial circuit includes
> simulating the serial circuit for a plurality of cycles as required to produce one output represented by the plurality of parallel equations,"

as recited in claim 1.

In the rejection of claim 1, the Office Action states that Foxcroft teaches "storing a plurality of 'strings' of data in a plurality of storage elements... where the plurality of 'strings' represent a plurality of initial values of a circuit." Office Action, p. 6. The Examiner states that items 70, 60, 62, 64, and 66 of FIG. 7 are storage elements that store 'strings.' As noted in lines 11-17 of col. 4 of Foxcroft, these items (registers R1-R5 of FIG. 7) are used to store the following values: "R1 is the Shift Register containing Syndrome bytes produced by the previous Syndrome block; R2 contains a locator polynomial $\Lambda(x)$, with $\Lambda_0=1$; R3 contains the D polynomial; R4 contains an evaluator polynomial $\Omega(x)$, with $\Omega_0=1$, and R5 is temporary storage for the A polynomial." Foxcroft neither teaches nor suggests that any of these structures store ASCII strings that represent initial values of a serial circuit, as recited in claim 1. Instead, Foxcroft simply teaches that these structures can be used to store syndrome bytes and A, D, locator, and evaluator polynomials.

The Office Action also states that Foxcroft teaches "storing the 'strings' in data structures... where the 'strings' represent mathematical operations." Office Action, p. 6. The

Office Action cites FIG. 1, most of cols. 4 and 6, and all of cols. 7-10 of Foxcroft as teaching these features. Applicant notes that, under 37 C.F.R. §1.104(c)(2), "The examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable." Applicant respectfully request that the Examiner more clearly point out which portion of FIG. 1 and cols. 4 and 6-10 is being relied upon in the rejection of claim 1. The Examiner appears to be relying on the data structures used in the hardware description language examples provided in cols. 8-9 of Foxcroft. However, none of these data structures store ASCII strings that represent one or more mathematical operations in the serial circuit, as recited in claim 1. Instead, these data structures are used to store various values such as inputs, outputs, and values generated by performing the mathematical operations that are expressly coded into the hardware description.

As the above discussion shows, Foxcroft fails to teach or suggest "storing a plurality of ASCII strings in each of a plurality of storage elements, wherein the plurality of ASCII strings represent a plurality of initial values of the serial circuit, [and] storing one or more ASCII strings in each of one or more data structures wherein the one or more ASCII strings represent one or more mathematical operations in the serial circuit," as recited in claim 1. None of the other cited art, either alone or in combination with Foxcroft, teaches or suggests these features. Accordingly, claim 1 is patentable over the cited art for at least the foregoing reasons.

Furthermore, the cited art fails to teach or suggest "simulating the serial circuit to produce a plurality of parallel equations, wherein simulating the serial circuit includes simulating the serial circuit for a plurality of cycles as required to produce one output represented by the plurality of parallel equations," as recited in claim 1. As noted by the Examiner on page 6 of the Office Action, Foxcroft does not teach this feature of claim 1. The Examiner relies on Oskouy to teach this feature, stating that Oskouy "discloses simulation of a serial device, using a hardware description language and simulating forward error correction (CRC) calculation." Office Action, p. 6.

Oskouy recites, in part:

> FIG. 4 illustrates a more detailed embodiment of the present invention. All of the components illustrated herein are simulated hardware. In this exemplary embodiment, network transporter 310 is under test. A packet is

> posted by simulated host system 312 and at the same time the packet's unique information is stored in TX pseudo FIFO 314. The posting is performed by packet poster 400. Cell generator 408 is invoked through a Verilog task (or any other feasible hardware simulator) to generate cells to network transporter 310 through simulated physical environment 316. Packet grabber 410 helps in capturing data of SBus which is used in validating the RX packets. Once a packet is transmitted to simulated physical layer 316, it is grabbed by cell grabber 402. Cell grabber 402 collects all cells transmitted from the external memory buffer 319 and performs CRC calculations on the entire packet and then compares the CRC with the CRC placed in TX pseudo FIFO 318 and the CRC calculated by network transporter 310 for error checking. In an exemplary embodiment, network transporter 310 may be an SBus ATM host interface to a single chip designed to connect an ATM interface to the host memory through an SBus. The unique information for the cell is sent to comparator 404 from TX pseudo FIFO 314. Since TX pseudo-FIFO 314 is a "pseudo" FIFO as described earlier, in one embodiment of the present invention, a packet information grabber may be implemented on the simulated host memory 312 side as well as the simulated physical layer side 316. Such packet information grabber (not shown) walks through the appropriate pseudo-FIFO and grabs the packet of information corresponding to the packet information grabbed by cell grabber 402 or packet grabber 410. The packet information grabber forms this task by checking the flag for each packet of information in the pseudo-FIFO which indicates whether or not the corresponding packet of information has been processed by the receiving process (simulated host memory 312 or simulated physical layer 316). The packet information skips over any packet of information entry which has already been processed and grabs the appropriate unprocessed packet of information corresponding to the packet of information grabbed by cell grabber 402. Comparator 404 then compares the unique information with the corresponding information in the packet to determine whether or not the test result is a pass or a fail. Oskouy, col. 4, line 53 - col. 5, line 27.

This portion of Oskouy describes using simulation to verify a network transporter using a simulated physical environment. However, the simulation techniques taught in Oskouy are used to test a network transporter, not a serial circuit that is implemented in a software program by, among other things, storing ASCII strings of the type recited in claim 1. Thus, Oskouy is simulating a different type of circuit than is recited in claim 1. Furthermore, the result of the simulation taught in Oskouy is that the proper operation of network transporter 310 can be verified, not the production of one or more parallel equations. Thus, while Oskouy does teach simulating a circuit, Oskouy does not teach simulating a serial circuit to produce a plurality of

parallel equations, as recited in claim 1. None of the other cited art, either alone or in combination with Oskouy, teaches or suggests this feature of claim 1.

Furthermore, the suggested combination of the references does not result in the claimed invention. The Office Action states: "It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have simulated the circuit design created using a hardware description language, as disclosed in the Foxcroft reference because the simulation will allow the designed [sic] to "Debug" the design before the design is fabricated." Office Action, p. 6. Applicant notes that simulating a circuit design for verification purposes will not "produce a plurality of parallel equations," as recited in claim 1.

For at least the foregoing reasons, claim 1 is patentable over the cited art. Claims 2-5 are patentable for at least the foregoing reasons provided above with respect to claim 1. Claims 8-25 are patentable over the cited art for similar reasons.

Claims 27-30, 32, 34-35, 37-40, 42, 44, and 45 were rejected under 35 U. 35 U.S.C. § 103(a) as being unpatentable over Tomizawa in view of Foxcroft. Applicant respectfully traverses this rejection. Dependent claims 27-30, 32, 34-35, 37-40, 42, 44, and 45 are patentable over the cited art for at least the foregoing reasons provided above with respect to independent claims 26 and 36.

Claims 33 and 43 were rejected under 35 U. 35 U.S.C. § 103(a) as being unpatentable over Tomizawa in view of Foxcroft in further view of Oskouy. Applicant respectfully traverses this rejection. Dependent claims 33 and 43 are patentable over the cited art for at least the foregoing reasons provided above with respect to independent claims 26 and 36.

Claims 31 and 41 were rejected under 35 U. 35 U.S.C. § 103(a) as being unpatentable over Tomizawa in view of Foxcroft in further view of Kao. Applicant respectfully traverses this rejection. Dependent claims 31 and 41 are patentable over the cited art for at least the foregoing reasons provided above with respect to independent claims 26 and 36.

CONCLUSION

In view of the amendments and remarks set forth herein, the application and the claims therein are believed to be in condition for allowance without any further examination and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5087.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, COMMISSIONER FOR PATENTS, P. O. Box 1450, Alexandria, VA 22313-1450, on November 30, 2004.

Brenna A Brock — 11-30-2004

Attorney for Applicant(s) — Date of Signature

Respectfully submitted,

Brenna A Brock

Brenna A. Brock
Attorney for Applicants
Reg. No. 48,509
(512) 439-5087 [Phone]
(512) 439-5099 [Fax]